UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/275,527	03/24/1999	DAVID KARCHMER	ALTRP049/A44	9876

22434 7590 01/07/2003

BEYER WEAVER & THOMAS LLP
P.O. BOX 778
BERKELEY, CA 94704-0778

EXAMINER
CRAIG, DWIN M

ART UNIT	PAPER NUMBER
2123	13

DATE MAILED: 01/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/275,527	Applicant(s) KARCHMER ET AL.	
	Examiner Dwin M Craig	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1- 28 have been presented for examination. Claims 1-28 have been examined and rejected.

Information Disclosure Statement

2. It is noted that the applicants have not provided an Information Disclosure Statement. Applicant is reminded of their duty to disclose all informational material to the patentability of the application as per 37 C.F.R. 1.56. Please note that in the specification the following reference is cited, *"Assignment Decision Diagrams for High-Level Synthesis" by Viraphol Chaiyakul and Daniel D. Gajski, Technical Report #92-102, December 12, 1992 see page 15, Lines 14-17,* the Examiner requires this material in order to review the application.

Drawings

3. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal Drawings will be required when the application is allowed. The drawings filed on 24 March 1999 are acceptable subject to correction of the formalities listed in the attached "Notice of Draft person's Patent Drawing Review," PTO-948.

4. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 19 May 1998 in applicant's provisional U.S. Patent Application No. 60/086,153 have been disapproved because they introduce new matter into the drawings. 37 CFR 1.121(a)(6) states that no amendment may introduce new matter into the disclosure of an application. The original

disclosure does not support the showing of the elements that are disclosed in Applicant's drawings submitted on 24 March 1999.

Specification

5. The attempt to incorporate subject matter into this application by reference *("Assignment Decision Diagrams for High-Level Synthesis" by Viraphol Chaiyakul and Daniel D. Gajski, Technical Report #92-102, December 12, 1992 see page 15, Lines 14-17 of Applicants Specification)* is improper because;

> The incorporation of essential material in the specification by reference to a foreign application or patent, or to a publication is improper. Applicant is required to amend the disclosure to include the material incorporated by reference. The amendment must be accompanied by an affidavit or declaration executed by the applicant, or a practitioner representing the applicant, stating that the amendatory material consists of the same material incorporated by reference in the referencing application. See *In re Hawkins*, 486 F.2d 569, 179 USPQ 157 (CCPA 1973); *In re Hawkins*, 486 F.2d 579, 179 USPQ 163 (CCPA 1973); and *In re Hawkins*, 486 F.2d 577, 179 USPQ 167 (CCPA 1973).

...as per the MPEP paragraph 6.19.

6. The amendment to the specification ,as compared to the priority document (provisional U.S. Patent Application No. 60/086,153 filed on 24 March 1999), is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure, the priority document, is as follows: **Figures 1-**

16, Specification (pages 1-34) and the Claims submitted on 24 March 1999 in the Non-Provisional Application number 09/275527.

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 1-28 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. All of the figures and written descriptions were not disclosed in Applicant's original provisional U.S. Patent Application No. 60/086,153 filed on 19 May 1998, and therefore the non-provisional application is new matter and as such is non-enabling for Claims 1-28.

Claim Interpretation

8. The claims have been given the broadest interpretation by the examiner. For the purposes of examination the examiner has determined that the term *non-atomic* refers to Hardware Description Language (HDL) source code that is used in a behavioral circuit simulation.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. **Claims 1, 2 and 6** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chang et al. U.S. Patent 6,269,467** in view of **"Assignment Decision Diagram for High Level Synthesis" by Viraphol Chaiykul and Daniel D. Gajski** here after referred to as the *Chaiykul et al.* reference, and in further view of **Seawrite et al. U.S. Patent 5,920,711.**

As regards **Claims 1** the *Chang et al.* reference discloses a behavioral model **(Figures 6, 9, 15, 25, 42, 69 and Col. 7 Lines 10-13, Col. 52 Lines 29-38)** and non-atomic behavioral simulation of process blocks in an electronic design **(Figures 1, 4, 5, 8-12, 29-31, 36, 37 and Col. 12 Lines 46-65),** receiving hardware design code describing a process block **(Col. 51 Lines 29-42).**

The *Chang et al.* reference does not expressly disclose, converting the hardware design code describing the process block to an assignment decision diagram (ADD) representation that is used to simulate behavior of the process block and including one or more control nodes for maintaining control flow through the simulator, thereby creating one or more break points that allow the simulator to stop at associated points in the process block.

The *Chaiykul et al.* reference discloses converting the hardware design code describing the process block to an assignment decision diagram (ADD) representation that is used to

simulate behavior of the process block and including one or more control nodes for maintaining control flow through the simulator, **(Pages 10-24).**

It would have been obvious to on of ordinary skill in the art, at the time of the invention, to have combined the *Chang et al.* reference with the *Chaiykul et al.* reference because, by using Assignment Decision Diagrams the designer has the ability for estimating layout quality metrics during synthesis tasks such as allocation and scheduling ***(Chaiykul et al. Page 25).***

The *Chang et al.* reference does not expressly disclose creating one or more break points that allow the simulator to stop at associated points in the process block.

The *Seawright et al.* reference teaches, creating one or more break points that allow the simulator to stop at associated points in the process block **(Figure 44, Items 4460 and 4470, and Figure 45b).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Seawright et al.* reference with the *Chang et al.* reference because a designer would like to be able to debug the design at the protocol level of abstraction ***(Seawrite et al. Col. 2 Lines 47-50).***

As regards **Claim 2** the *Chang et al.* reference does not expressly disclose assignment decision diagrams.

The *Chaiykul et al.* reference discloses assignment decision diagrams **(Pages 1-49).**

It would have been obvious to on of ordinary skill in the art, at the time of the invention, to have modified the *Chang et al.* reference with the *Chaiykul et al.* reference because, by using Assignment Decision Diagrams the designer has the ability for estimating layout quality metrics during synthesis tasks such as allocation and scheduling ***(Chaiykul et al. Page 25).***

As regards **Claim 6** the *Chang et al.* reference does not expressly disclose, VHDL or Verilog.

The *Seawright et al.* reference teaches VHDL or Verilog **(Figure 59, Item 2706).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have combined the *Seawright et al.* reference with the *Chang et al.* reference because a designer would like to be able to debug the design at the protocol level of abstraction ***(Seawrite et al. Col. 2 Lines 47-50).***

10. **Claims 3, 4 and 5** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chang et al. U.S. Patent 6,269,467** in view of **"Assignment Decision Diagram for High Level Synthesis" by Viraphol Chaiykul and Daniel D. Gajski** here after referred to as the *Chaiykul et al.* reference, and in further view of **Seawrite et al. U.S. Patent 5,920,711** and in further view of **McGeer et al. U.S. Patent 6,421,808.**

As regards all of independent **Claim 1's** limitations, were addressed in paragraph 9 above.

The *Chang et al.* reference does not expressly disclose, control nodes, conditional branches in a control flow, a suspend control node, a block token, a parse tree, traversing a parse tree and maintaining control flow through a simulator.

As regards **Claim 3** the *Chang et al.* reference does not expressly disclose;

A control node being selected from a group of control nodes,

The selected control node representing a conditional branch in the control flow of the simulation,

A null control node used as a place holder,

A suspend node used to suspend execution of a process block.

The *McGeer et al.* reference discloses control nodes and groups of control nodes, the selected control node representing a conditional branch in the control flow of the simulation, a null control node used as a place holder, a suspend node used to suspend execution of a process block **(Figure 11, 14-17, 28 and Col. 2 Lines 56-57, Col. 36 Lines 17-20, Figure 11-24, Col. 22 Lines 52-67, Col. 23 Lines 25-50, Col. 33-41).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Chang et al.* reference with the *McGeer et al.* reference because, V++ introduces little resource overhead. In addition the shorter design cycle and smaller resource sizes can benefit large designs, improve maintainability, and provide correct designs more quickly ***(McGeer et al. Col. 51 Lines 65-67 and Col. 52 Lines 1-3).***

As regards **Claim 4** the *Chang et al.* reference does not expressly disclose;

The suspend control node is selected from a group comprising an event type suspend control node used to suspend execution of the process block pending a pre-determined future event and a delay type suspend control node used to suspend execution of the process block for a specified length of time.

The *McGeer et al.* reference discloses, the suspend control node is selected from a group comprising an event type suspend control node used to suspend execution of the process block, **(Figure 11, 14-17, 28 and Col. 2 Lines 56-57, Col. 36 Lines 17-20, Figure 11-24, Col. 22 Lines 52-67, Col. 23 Lines 25-50, Col. 33-41).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Chang et al.* reference with the *McGeer et al.* reference because, V++ introduces little resource overhead. In addition the shorter design cycle and smaller resource sizes can benefit large designs, improve maintainability, and provide correct designs more quickly ***(McGeer et al. Col. 51 Lines 65-67 and Col. 52 Lines 1-3).***

The *Chang et al.* reference does not expressly disclose pending a pre-determined future event and a delay type suspend control node used to suspend execution of the process block for a specified length of time.

The *Seawrite et al.* reference discloses, pending a pre-determined future event and a delay type suspend control node used to suspend execution of the process block for a specified length of time **(Figure 16, 23, 24, 25, 26, 34, 44, 45a, 45b, 45c).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Seawright et al.* reference with the *Chang et al.* reference because a designer would like to be able to debug the design at the protocol level of abstraction ***(Seawrite et al. Col. 2 Lines 47-50).***

As regards **Claim 5** the *Chang et al.* reference does not expressly disclose;

Synthesizing a circuit level parse tree upon operational characteristics and schematic layout of the circuit being simulated contained within the hardware design code, wherein the parse tree includes a process token and a process block token, the process token identifying a simulation process to be carried out within the process block;

Traversing the parse tree and allocating a process block structure in the simulation object file when the process block token is encountered.

Further traversing the parse tree to determine if the process token is available.

Determining the type of simulation process identified by the process token.

Converting the identified simulation process to a corresponding ADD.

Annotating the ADD with a plurality of selected control nodes that are responsible for control flow through the simulator wherein each of the control nodes has a pointer and the control nodes are stored in a list.

The *McGeer et al.* reference discloses; Synthesizing a circuit level parse tree upon operational characteristics and schematic layout of the circuit being simulated contained within the hardware design code, wherein the parse tree includes a process token and a process block token, the process token identifying a simulation process to be carried out within the process block;

Traversing the parse tree and allocating a process block structure in the simulation object file when the process block token is encountered.

Further traversing the parse tree to determine if the process token is available.

Determining the type of simulation process identified by the process token.

(Figures 14-29, Col. 30 Lines 20-67, All of Columns 31-50, Col. 51 Lines 1-63).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Chang et al.* reference with the *McGeer et al.* reference because, V++ introduces little resource overhead. In addition the shorter design cycle and smaller resource sizes can benefit large designs, improve maintainability, and provide correct designs more quickly ***(McGeer et al. Col. 51 Lines 65-67 and Col. 52 Lines 1-3).***

The *Chang et al.* reference does not expressly disclose, Converting the identified simulation process to a corresponding ADD, annotating the ADD with a plurality of selected control nodes that are responsible for control flow through the simulator wherein each of the control nodes has a pointer and the control nodes are stored in a list.

The *Chaiykul et al.* reference discloses Converting the identified simulation process to a corresponding ADD, annotating the ADD with a plurality of selected control nodes that are responsible for control flow through the simulator wherein each of the control nodes has a pointer and the control nodes are stored in a list **(Pages 1-49).**

It would have been obvious to on of ordinary skill in the art, at the time of the invention, to have modified the *Chang et al.* reference with the *Chaiykul et al.* reference because, by using Assignment Decision Diagrams the designer has the ability for estimating layout quality metrics during synthesis tasks such as allocation and scheduling ***(Chaiykul et al. Page 25).***

11. **Claims 7 and 8** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chang et al. U.S. Patent 6,269,467** in view of **"Assignment Decision Diagram for High Level Synthesis" by Viraphol Chaiykul and Daniel D. Gajski** here after referred to as the *Chaiykul et al.* reference, and in further view of **Seawrite et al. U.S. Patent 5,920,711.**

As regards **Claims 7 and 8** the *Chang et al.* reference discloses a behavioral model **(Figures 6, 9, 15, 25, 42, 69 and Col. 7 Lines 10-13, Col. 52 Lines 29-38)** and non-atomic behavioral simulation of process blocks in an electronic design **(Figures 1, 4, 5, 8-12, 29-31, 36,**

37 and Col. 12 Lines 46-65), receiving hardware design code describing a process block **(Col. 51 Lines 29-42).**

As regards **Claim 7,** the *Chang et al.* reference does not expressly disclose, converting the hardware design code describing the process block to an assignment decision diagram (ADD) representation that is used to simulate behavior of the process block and including one or more control nodes for maintaining control flow through the simulator, thereby creating one or more break points that allow the simulator to stop at associated points in the process block.

The *Chaiykul et al.* reference discloses converting the hardware design code describing the process block to an assignment decision diagram (ADD) representation that is used to simulate behavior of the process block and including one or more control nodes for maintaining control flow through the simulator, **(Pages 10-24).**

It would have been obvious to on of ordinary skill in the art, at the time of the invention, to have combined the *Chang et al.* reference with the *Chaiykul et al.* reference because, by using Assignment Decision Diagrams the designer has the ability for estimating layout quality metrics during synthesis tasks such as allocation and scheduling ***(Chaiykul et al. Page 25).***

As regards **Claim 8** the *Chang et al.* reference does not expressly disclose, creating one or more break points that allow the simulator to stop at associated points in the process block.

The *Seawright et al.* reference teaches, creating one or more break points that allow the simulator to stop at associated points in the process block **(Figure 44, Items 4460 and 4470, and Figure 45b).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Chaiykul et al.* reference with the *Seawright et al.* reference because a

designer would like to be able to debug the design at the protocol level of abstraction ***(Seawrite et al. Col. 2 Lines 47-50).***

12. **Claims 9 and 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chang et al. U.S. Patent 6,269,467** in view of **"Assignment Decision Diagram for High Level Synthesis" by Viraphol Chaiykul and Daniel D. Gajski** here after referred to as the *Chaiykul et al.* reference, and in further view of **Seawrite et al. U.S. Patent 5,920,711** and in further view of **McGeer et al. U.S. Patent 6,421,808.**

As regards all of independent **Claim 7's** limitations, were addressed in paragraph 11 above.

As regards **Claim 9** the *Chang et al.* reference does not expressly disclose; the control node being selected from a group of query control nodes used to represent conditional branches in control flow, an evaluation/assignment control node used to represent an assignment operation, a null control node used as a place holder, and a suspend control node used to suspend execution of the process block.

The *McGeer et al.* reference discloses; the control node being selected from a group of query control nodes used to represent conditional branches in control flow, an evaluation/assignment control node used to represent an assignment operation, a null control node used as a place holder, and a suspend control node used to suspend execution of the process block **(Figure 11, 14-17, 28 and Col. 2 Lines 56-57, Col. 36 Lines 17-20, Figure 11-24, Col. 22 Lines 52-67, Col. 23 Lines 25-50, Col. 33-41).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Chang et al.* reference with the *McGeer et al.* reference because, V++ introduces little resource overhead. In addition the shorter design cycle and smaller resource sizes can benefit large designs, improve maintainability, and provide correct designs more quickly ***(McGeer et al. Col. 51 Lines 65-67 and Col. 52 Lines 1-3).***

As regards **Claim 10** the *Chang et al.* reference does not expressly disclose; the suspend control node is selected from the group comprising an event type suspend control node used to suspend execution of the process block pending a pre-determined future event and a delay type suspend control node used to suspend execution of the process block for a specific length of time.

The *Seawrite et al.* reference discloses, an event type suspend control node used to suspend execution of the process block pending a pre-determined future event and a delay type suspend control node used to suspend execution of the process block for a specific length of time **(Figure 16, 23, 24, 25, 26, 34, 44, 45a, 45b, 45c).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Seawright et al.* reference with the *Chang et al.* reference because a designer would like to be able to debug the design at the protocol level of abstraction ***(Seawrite et al. Col. 2 Lines 47-50).***

13. **Claims 11-25** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Gregory et al. U.S. Patent 5,937,190** in view of **Gregory U.S. Patent 5,870,608** and in further view of **"Assignment Decision Diagram for High Level Synthesis" by Viraphol Chaiykul and**

Daniel D. Gajski here after referred to as the *Chaiykul et al.* reference and in further view of **McGeer et al. U.S. Patent 6,421,808.**

As regards **Claim 11** the *Gregory et al.* reference discloses a method of compiling a simulation object file to simulate the operation of a digital circuit **(Figure 1, 3 Item 154, Col. 6 Lines 37-64),** wherein the simulation object file represents a behavioral model process block arranged to simulate the operation of the digital circuit by providing an output signal based on the input signal **(Figures 4-8, 43-44, Col. 3 Lines 9-21)** comprising;

(a) A parse tree, which includes a token, and a token based hierarchy, wherein the token identifies a process block wherein there is code describing the circuit being simulated, **(Figures 2-12, Figure 58 Item 6004, specifically, Figure 5-bottom of figure, Col. 11 Lines 4-15).**

(b) Traversing the parse tree and allocating a process block structure in the simulation object file when a token is encountered **(Figures 5-9, 35, 36, 39, 60 and Col. 8 Lines 60-68, Col. 9 Lines 1-46, Col. 17 Lines 11-31, Col. 21 Lines 1-4, Col. 21 Lines 35-56, Col. 25 Lines 45-58),**

(d) Determining the type of simulation process identified by the token **(Col. 18 Lines 49-62, Col. 3 Lines 22-37).**

The *Gregory et al.* reference does not expressly disclose,

(c) Further traversing the parse tree to find an available token.

(e) Converting the simulation process to an assignment decision diagram.

(f) Annotating the assignment decision diagram with a plurality of selected control nodes which control the flow through the simulation, wherein said control nodes have a pointer to the next control node that is used to proceed through to the next step in the simulation process

wherein the control nodes are stored in a process block control node list contained in the object file.

The *Gregory* reference discloses;

(c) Further traversing the parse tree to find an available token **(Figure 4 Item 1009).**

...a plurality of selected control nodes which control the flow through the program, wherein said control nodes have a pointer to the next control node that is used to proceed through to the next step in the process wherein the control nodes are stored in a process block control node list contained in the object file **(Figures 1, 4-6, and Col. 3 Lines 26-67, Col. 4 Lines 1-44, Col. 10 Lines 50-67,Col. 51, 52, 69, 70, 71, 72, 85, 86, 87, 88, 95, 96, 117, 118, 125, 126, 129, 130,149, 150, 151, 152, 159, 160, 197, 198, 245, 246, 247, 248, 249, 250, 293, 294, all of 372, 373 and 374)**.

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Gregory et al.* reference with the *Gregory* reference because, the *Gregory* reference refers to the *Gregory et al.* reference in its specification ***(Gregory, Col. 8 Lines 28-38).***

The *Gregory et al.* reference does not expressly disclose, Converting the simulation process to an assignment decision diagram.

The *Chaiykul et al.* reference discloses Converting the simulation process to an assignment decision diagram **(Pages 10-24).**

It would have been obvious to on of ordinary skill in the art, at the time of the invention, to have modified the *Gregory et al.* reference with the *Chaiykul et al.* reference because, by

using Assignment Decision Diagrams the designer has the ability for estimating layout quality metrics during synthesis tasks such as allocation and scheduling ***(Chaiykul et al. Page 25).***

The *Gregory et al.* reference discloses sub-parse trees **(Figure 9, Items 39101, 39103, 39102, 39104, 39105 and 39106.**

As regards **Claim 13** the *Gregory et al.* reference does not expressly disclose, an assignment decision diagram, an assignment value portion assigned to an output port, as assignment condition connected to a data flow path such that the end condition is either TRUE or FALSE, an assignment decision node.

The *Chaiykul et al.* reference discloses an assignment decision diagram, an assignment value portion assigned to an output port, as assignment condition connected to a data flow path such that the end condition is either TRUE or FALSE, an assignment decision node **(Pages 1-49).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Gregory et al.* reference with the *Chaiykul et al.* reference because, by using Assignment Decision Diagrams the designer has the ability for estimating layout quality metrics during synthesis tasks such as allocation and scheduling ***(Chaiykul et al. Page 25).***

As regards **Claim 14,** the *Gregory et al.* reference does not expressly disclose, a control node selected from a group of query control node used to represent a conditional branch in a control flow, an evaluation/assignment control node used to represent an assignment operation, a null control node used as a place holder and a suspend control node used to suspend execution of a process block.

The *McGeer et al.* reference discloses, a control node selected from a group of query control node used to represent a conditional branch in a control flow **(Figure 11, 14-17, 28 and Col. 2 Lines 56-57, Col. 36 Lines 17-20),** an evaluation/assignment control node used to represent an assignment operation, a null control node used as a place holder and a suspend control node used to suspend execution of a process block, **(Figure 11-24, Col. 22 Lines 52-67, Col. 23 Lines 25-50, Col. 33-41).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Gregory et al.* reference with the *McGeer et al.* reference because, V++ introduces little resource overhead. In addition the shorter design cycle and smaller resource sizes can benefit large designs, improve maintainability, and provide correct designs more quickly ***(McGeer et al. Col. 51 Lines 65-67 and Col. 52 Lines 1-3).***

As regards **Claims 15 and 16** the *Gregory et al.* reference discloses a suspend node with an event type suspend control node used to suspend execution of the process block pending a pre-determined future event and wherein the suspend node comprises; a delay type suspend control node to suspend execution of the process block for a specific length of time. **(Col. 21 Lines 18-67, Col. 22 Lines 1-67).**

As regards to **Claim 17,** the *Gregory et al.* reference does not expressly disclose, pointers and tokens.

The *Gregory* reference discloses pointers and tokens **(Figures 1, 4-6, and Col. 3 Lines 26-67, Col. 4 Lines 1-44, Col. 10 Lines 50-67,Col. 51, 52, 69, 70, 71, 72, 85, 86, 87, 88, 95, 96, 117, 118, 125, 126, 129, 130,149, 150, 151, 152, 159, 160, 197, 198, 245, 246, 247, 248, 249, 250, 293, 294, all of 372, 373 and 374).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Gregory et al.* reference with the *Gregory* reference because, the *Gregory* reference refers to the *Gregory et al.* reference in its specification ***(Gregory, Col. 8 Lines 28-38).***

As regards **Claim 18** the *Gregory et al.* reference does not expressly disclose, converting a true sub-parse tree to a true conditional ADD and converting false sub-parse tree to a corresponding false conditional ADD.

The *Chaiykul et al.* reference discloses converting a true sub-parse tree to a true conditional ADD and converting false sub-parse tree to a corresponding false conditional ADD **(Pages 1-49).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Gregory et al.* reference with the *Chaiykul et al.* reference because, by using Assignment Decision Diagrams the designer has the ability for estimating layout quality metrics during synthesis tasks such as allocation and scheduling ***(Chaiykul et al. Page 25).***

As regards **Claim 19** the *Gregory et al.* reference does not expressly disclose mapping the control nodes.

The *Gregory* reference discloses mapping the control nodes **(Col. 372 Lines 48-67 and Col. 373 Lines 1-2).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Gregory et al.* reference with the *Gregory* reference because, the *Gregory* reference refers to the *Gregory et al.* reference in its specification ***(Gregory, Col. 8 Lines 28-38).***

As regards **Claim 20** the *Gregory et al.* reference does not expressly disclose, a process loop type token, the loop process having a loop entry condition and a loop exit condition suitable

for entering and exiting a corresponding loop expression and loop body, allocating a query control node to the process control node list.

The *McGeer et al.* reference discloses a process loop type token, the loop process having a loop entry condition and a loop exit condition suitable for entering and exiting a corresponding loop expression and loop body, allocating a query control node to the process control node list **(Figure 22, Col. 25 Lines 6-67, Col. 26 Lines 1-36, Col. 37 Lines 40-51, Col. 39 Lines 48-67, Col. 40 Lines 1-67, Col. 41 Lines 1-5).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Gregory et al.* reference with the *McGeer et al.* reference because, V++ introduces little resource overhead. In addition the shorter design cycle and smaller resource sizes can benefit large designs, improve maintainability, and provide correct designs more quickly ***(McGeer et al. Col. 51 Lines 65-67 and Col. 52 Lines 1-3).***

The *Gregory et al.* reference does not expressly disclose, converting loop expression sub-parse tree to a corresponding loop expression ADD and recursively converting the loop body sub-parse tree to a loop body ADD.

The *Chaiykul et al.* reference discloses converting loop expression sub-parse tree to a corresponding loop expression ADD and recursively converting the loop body sub-parse tree to a loop body ADD **(Pages 1-49).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Gregory et al.* reference with the *Chaiykul et al.* reference because, by using Assignment Decision Diagrams the designer has the ability for estimating layout quality metrics during synthesis tasks such as allocation and scheduling ***(Chaiykul et al. Page 25).***

As regards **Claim 21** the *Gregory et al.* reference does not expressly disclose, pointers, control nodes and mapping.

The *McGeer et al. reference* discloses pointers, control nodes and mapping **(Figures 14, 15 and 35, Col. 5 Lines 40-54).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Gregory et al.* reference with the *McGeer et al.* reference because, V++ introduces little resource overhead. In addition the shorter design cycle and smaller resource sizes can benefit large designs, improve maintainability, and provide correct designs more quickly ***(McGeer et al. Col. 51 Lines 65-67 and Col. 52 Lines 1-3).***

The *Gregory et al.* reference does not expressly disclose, mapping the control node to an ADD.

The *Chaiykul et al.* reference discloses mapping the control node to an ADD **(Pages 1-49).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Gregory et al.* reference with the *Chaiykul et al.* reference because, by using Assignment Decision Diagrams the designer has the ability for estimating layout quality metrics during synthesis tasks such as allocation and scheduling ***(Chaiykul et al. Page 25).***

As regards **Claims 22 and 23** the *Gregory et al.* reference does not expressly disclose, a suspend token.

The *McGeer et al.* reference discloses a suspend token **(Col. 21 Lines 43-67).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Gregory et al.* reference with the *McGeer et al.* reference because, V++

introduces little resource overhead. In addition the shorter design cycle and smaller resource sizes can benefit large designs, improve maintainability, and provide correct designs more quickly ***(McGeer et al. Col. 51 Lines 65-67 and Col. 52 Lines 1-3).***

The *Gregory et al.* reference does not expressly disclose, converting the control node to an ADD.

The *Chaiykul et al.* reference discloses converting the control node to an ADD **(Pages 1-49).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Gregory et al.* reference with the *Chaiykul et al.* reference because, by using Assignment Decision Diagrams the designer has the ability for estimating layout quality metrics during synthesis tasks such as allocation and scheduling ***(Chaiykul et al. Page 25).***

As regards **Claims 24 and 25** the *Gregory et al.* reference does not expressly disclose, converting the control node to an ADD.

The *Chaiykul et al.* reference discloses converting the control node to an ADD **(Pages 1-49).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Gregory et al.* reference with the *Chaiykul et al.* reference because, by using Assignment Decision Diagrams the designer has the ability for estimating layout quality metrics during synthesis tasks such as allocation and scheduling ***(Chaiykul et al. Page 25).***

The *Gregory et al.* reference does not expressly disclose, pointers, control nodes and mapping.

The *McGeer et al. reference* discloses pointers, control nodes and mapping **(Figures 14, 15 and 35, Col. 5 Lines 40-54),** allocating a query control node to the process control node list **(Figure 22, Col. 25 Lines 6-67, Col. 26 Lines 1-36, Col. 37 Lines 40-51, Col. 39 Lines 48-67, Col. 40 Lines 1-67, Col. 41 Lines 1-5).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Gregory et al.* reference with the *McGeer et al.* reference because, V++ introduces little resource overhead. In addition the shorter design cycle and smaller resource sizes can benefit large designs, improve maintainability, and provide correct designs more quickly **(McGeer et al. Col. 51 Lines 65-67 and Col. 52 Lines 1-3).**

As regards **Claim 26** the *Gregory et al.* reference discloses a Field Programmable Gate Array **(Col. 1 Lines 33-51).**

14. **Claims 27 and 28** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Dearth et al. U.S. Patent 5,848,236** in view of **Gregory et al. U.S. Patent 5,937,190** and in further view of **"Assignment Decision Diagram for High Level Synthesis" by Viraphol Chaiykul and Daniel D. Gajski** here after referred to as the *Chaiykul et al.* reference.

As regards **Claim 27** the *Dearth et al.* reference discloses, A computer program project **(Col. 1 Lines 45-63)** comprising computer program instructions **(Col. 3 Lines 15-46, Col. 6 Lines 52-65)** provided on a computer readable medium **(Col. 5 Lines 43-61)**, specifying a method of compiling a simulation object **(Col. 6 Lines 66-67 and Col. 7 Lines 1-67)** used by a simulator to simulate the operation of a digital circuit **(Col. 1 Lines 35-42).**

The *Dearth et al.* reference does not expressly disclose, a behavioral model process block, synthesizing a circuit level parse tree with a process token, traversing the parse tree and allocating a process block when the token is encountered, determining the type of simulation from the token, converting the identified simulation process to a corresponding assignment decision diagram, and annotating the assignment decision diagram (ADD) with control nodes that control flow through the simulator with pointers, wherein the pointers are stored in a process block control node list contained in the object file.

The *Gregory et al.* reference discloses, a behavioral model process block **(Figure 2, Col. 1 Lines 15-20)** synthesizing a circuit level parse tree with a process token **(Figure 58 Item 6004, Figure 5-bottom of figure),** traversing the parse tree and allocating a process block when the token is encountered, determining the type of simulation from the token, **(Figures 5-9, 35, 36, 39, 60 and Col. 8 Lines 60-68, Col. 9 Lines 1-46, Col. 17 Lines 11-31, Col. 21 Lines 1-4, Col. 21 Lines 35-56, Col. 25 Lines 45-58),** with control nodes that control flow through the simulator with pointers, wherein the pointers are stored in a process block control node list contained in the object file **(Col. 8 Lines 49-59).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Dearth et al.* reference with the *Gregory et al.* reference because, There has been a need for a system that allows the designer to analyze a digital circuit design in terms of the source HDL. ***(Gregory et al. Col. 8 lines 33-35).***

The *Dearth et al.* reference does not expressly disclose, converting the hardware design code describing the process block to an assignment decision diagram (ADD) representation that

is used to simulate behavior of the process block and including one or more control nodes for maintaining control flow through the simulator.

The *Chaiykul et al.* reference discloses converting the hardware design code describing the process block to an assignment decision diagram (ADD) representation that is used to simulate behavior of the process block and including one or more control nodes for maintaining control flow through the simulator, **(Pages 10-24).**

It would have been obvious to on of ordinary skill in the art, at the time of the invention, to have modified the *Dearth et al.* reference with the *Chaiykul et al.* reference because, by using Assignment Decision Diagrams the designer has the ability for estimating layout quality metrics during synthesis tasks such as allocation and scheduling ***(Chaiykul et al. Page 25).***

As regards **Claim 28** the *Dearth et al.* reference discloses an apparatus **(Figures 1, 2 and 19C, Col. 1 Lines 35-42)** and an editor **(Col. 6 Lines 43-53).**

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 9:00 - 5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-3900.

DMC
December 29, 2002

HUGH JONES Ph.D.
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2100